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(54) **MEMORY MODULE WITH A CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION**

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CPC ***G11C 5/04*** (2013.01); ***G06F 12/0207*** (2013.01); ***G06F 12/0215*** (2013.01); ***G11C 5/066*** (2013.01); ***G11C 7/1048*** (2013.01); ***G11C 8/12*** (2013.01); ***H05K 1/181*** (2013.01); *G11C 2207/105* (2013.01); *H05K 2201/10159* (2013.01); *H05K 2203/1572* (2013.01); *Y02B 60/1225* (2013.01); *Y02P 70/611* (2015.11)

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 95/001,381, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

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(57) **ABSTRACT**

A memory module includes a plurality of memory devices and a circuit. Each memory device has a corresponding load. The circuit is electrically coupled to the plurality of memory devices and is configured to be electrically coupled to a memory controller of a computer system. The circuit selectively isolates one or more of the loads of the memory devices from the computer system. The circuit comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.